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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/660,555	09/12/2003	Mitsuaki Izuha	04329.3139	6394
22852	7590	06/05/2006	EXAMINER	
FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER LLP 901 NEW YORK AVENUE, NW WASHINGTON, DC 20001-4413			HU, SHOUXIANG	
			ART UNIT	PAPER NUMBER
			2811	

DATE MAILED: 06/05/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary

Application No.

10/660,555

Applicant(s)

IZUHA ET AL.

Examiner

Shouxiang Hu

Art Unit

2811

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 15 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1 and 4-15 is/are pending in the application.
- 4a) Of the above claim(s) 7-14 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,4-6 and 15 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☒ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|-----------------------------------------------------------------------------------------|-----------------------------------------------------------------------------|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Pending Claims

According to the previous office actions and the latest amendment, claims 1 and 4-15 are pending in this application; and claims 1, 4-6 and 15 remain active in this office action.

Claim Objections

Claim 6 is objected to because of the following informalities and/or defects:

Claim 6 recites the subject matters that the lightly doped third and fourth impurity regions are formed in the first and second impurity diffusion region that are heavily doped, but it is not clear how the lightly doped regions could be formed in the heavily doped regions. The light doped regions are normally extended source/drain regions, but they are not parts of the heavily doped source/drain region; and any lightly doped region cannot be logically regarded also as a heavily doped region.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ku (Ku et al., High Performance pMOSFETs with Ni(Si_xGe_{1-x})/Poly-Si_{0.8}Ge_{0.2} Gate, 2000 Symposium on VLSI Technology Digest of Technical Papers, pages 114-115; of record) in view of Naruse (Naruse et al., US 5,356,821).

Ku discloses a semiconductor device (see the entire article, especially Figs. 1-11), having a MOSFET, the MOSFET being formed through a Ni-salicide process (see the abstract) which naturally comprising: source and drain regions formed in a major surface region of a semiconductor substrate; a gate insulating film formed on a channel region between the source and drain regions; a gate electrode which is formed on the gate insulating film and formed of a poly-Si_{1-x}Ge_x layer; a first metal silicide film which is formed on the gate electrode and essentially consists of NiSi_{1-y}Ge_y (see Fig. 8); and second and third metal silicide films which are formed on the source and drain regions, respectively, and essentially consist of NiSi (see Fig. 9).

Ku further discloses that the gate electrode of the poly-Si_{1-x}Ge_x layer has a Ge/(Si+Ge) composition ratio x of 0.2, which is substantially close to the upper limit of 0.16 as defined in claim 1 as amended.

Although Ku does not expressly disclose that the composition ratio x can be a little bit less than the above upper limit 0.16, it is noted that the composition ratio is an art-known result-oriented parameter of importance subject to routine experimentation and optimization, and that the composition ratio x of a little bit less than 0.16 is well within the art-known common range for a poly-Si_{1-x}Ge_x layer in the gate electrode, as readily evidenced in the prior art such as Naruse (see the abstract).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to make the device of Ku with the composition ratio x being a little bit less than 0.16 through routine experimentation, per the teachings of Naruse, so that a device with optimized performance for the MOSFET therein would be obtained.

Regarding claim 5, it is noted that the thickness of the poly-Si_{1-x}Ge_x layer in the gate electrode is substantially at least twice that of the first metal silicide film (see Fig. 3); and/or that the thicknesses of the two are both art-known result-oriented parameters of importance subject to routine experimentation and optimization.

Claims 4, 6 and 15, as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Ku in view of Kaneshiro (Kaneshiro et al., US 5,427,964) and/or Oda (US 6,288,430).

The disclosure of Ku is discussed as applied to claims 1 and 5 above.

Ku does not expressly disclose that the MOSFET in the device can further include contact structures each having a plug with a barrier layer overlying and connected to each of the gate electrode and the source and drain regions, and/or that the source and drain regions comprise the extensions and doped regions as recited in claim 6. However, one of ordinary skill in the art would readily recognize that such contact structures and/or such source and drain regions are each commonly formed in the art for establishing required and/or reliable contacts to the gate electrode and the source/drain regions, and/or for improving MOSFET performance with reduced short

Art Unit: 2811

channel effect, respectively, as evidenced in Kaneshiro (see the plugs 96, 101 and 102 in the interlayer dielectric film 54 in Figs. 13 and 14; also see the extended source and drain regions (88, 83, and 74), the lightly doped regions 83 and 84, and the heavily doped regions (at least the top portions of 88 and 89, which include additional dopants than the regions 83 and 84). And, as evidenced in Oda (Fig.3), it is art-known that a tungsten contact plug (35) protected with a TiN barrier layer (34) can be desirably formed for obtaining a reliable interconnection (also see the extended source and drain regions including the lightly doped regions 22 and the heavily doped regions 25).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the source/drain regions of Kaneshiro and/or Oda into the device collectively taught by Ku and Naruse, with contact plugs being formed of tungsten and protected with a TiN barrier layer respectively for the gate electrode and the source and drain regions, per the further teachings of Kaneshiro and/or Oda, so that a device with improved performance, and/or with desired and/or reliable interconnections, for the MOSFET therein would be obtained.

Response to Arguments

Applicant's arguments filed on March 15, 2006 have been fully considered but they are not persuasive.

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention

Art Unit: 2811

where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, Ku teaches the claimed invention except the recited Ge/(Si+Ge) composition ratio x of being less than 0.16. However, Ku does disclose that the composition ratio can be 0.2, which is substantially close to the upper limit of 0.16 recited in claim 1 as amended; and Naruse is cited to show that one of ordinary skill in the art would readily recognize that the composition ratio is an art-known result-oriented parameter of importance subject to routine experimentation and optimization, and that the composition ratio x of a little bit less than 0.16 is well within the art-known common range for a poly-Si_{1-x}Ge_x layer in the gate electrode. Accordingly, it would be well within the ordinary skill in the art to make the device of Ku with the composition ratio x being a little bit less than 0.16 through routine experimentation, per the teachings of Naruse, so as to achieved optimized performance for the MOSFET-comprised device, as it has been held that “[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.” *In re Aller*, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Furthermore, it is noted that the teachings of Naruse does not construe a teaching away from Ku, since it is Naruse itself that specifically teaches the range for the composition ratio for the gate electrode layer still covers the one of being a little bit less than 0.16, which is well within the art-known common range for a poly-Si_{1-x}Ge_x

layer in the gate electrode, even though Naruse already recognizes some benefit with higher composition ratio, and since it is the nature of the art to optimize the resulted-oriented composition ratio by considering various competing factors, benefits and/or side effects, instead of considering only one particular benefit.

Applicant alleges that unexpected results were achieved with the claimed range, but fails to provide adequate evidence to show why the claimed range is so critical and what were exactly expected and unexpected by the inventors at the time the instant invention was made, as it has been held that: "The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range." *In re Woodruff*, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). Applicant is encouraged to file a declaration to provide such evidence.

Regarding claim rejections relevant to claims 4, 6 and 15, it is noted that, in response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). And, in response to applicant's

Art Unit: 2811

arguments against the references individually, one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). In this case, Kaneshiro and/or Oda were cited to show that the recited features about the contact structures and about the impurity regions each are art-known features commonly utilized in the art with well-recognized expectations for the results, such as for establishing required and/or reliable contacts to the gate electrode and the source/drain regions, and/or for improving MOSFET performance with reduced short channel effect, respectively. And, the incorporation of such features into the device collectively taught by Ku and Naruse naturally results in the claimed invention as defined in this claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Thursday, 7:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>.

Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SH
May 25, 2006



SHOUXIANG HU
PRIMARY EXAMINER